

ABSTRACT

A non-volatile memory array has word lines coupled to floating gates, the floating gates having an upper portion that is adapted to provide increased surface area, and thereby, to provide increased coupling to the word lines. Shielding between floating gates is also provided. A first process forms floating gates by etching an upper portion of a polysilicon structure with masking elements in place to shape the floating gate. A second process etches recesses and protrusions in a polysilicon structure prior to etching the structure to form individual floating gates.